CLAIMS:

1. A circuit comprising:

a first data channel and at least one other channel;

clock synchronising means for generating a local clock synchronised with the first data channel;

timing means associated with the first data channel for measuring the time since the last data transition on that channel and operable to provide a timing signal indicative of that time;

phase detect means, associated with the first data channel, for detecting a representative phase of a selected set of one or more channels, that set comprising, at least, said at least one other channel;

phase adjustment means for adjusting the phase of the local clock in response to the timing signal towards said phase of said set.

2. A circuit as claimed in claim 1, wherein said set consists of a single channel, being the or one of said at least one other channel, and said representative phase is the phase of that single channel.

3. A circuit as claimed in claim 1, wherein said set comprises a plurality of channels.

4. A circuit as claimed in claim 3, wherein said phase representative of said set is an average of the phases of the members of said set.

5. A circuit as claimed in claim 3, wherein said set comprises said at least one other channel and said first data channel itself.

6. A circuit as claimed in claim 1, wherein the timing means is arranged to issue a first interval signal when a first time period has elapsed since a last data transition occurred on the first data channel.

7. A circuit as claimed in claim 1, wherein, in the continued absence of a data transition on the first data channel, the timing means is arranged to issue interval signals at constant intervals.

8. A circuit as claimed in claim 1, wherein in the continued absence of a data transition on the first data channel, the timing means is arranged to issue interval signals at intervals that get progressively shorter.

9. A circuit as claimed in claim 8, wherein the intervals are subject to a minimum time interval.

10. A circuit as claimed in claim 6, wherein the phase adjustment means is responsive to said interval signals to adjust the phase of the local clock towards the phase of said selected set.

11. A circuit as claimed in claim 10, wherein the phase adjustment means is responsive to successive interval signals to adjust the phase of the local clock by a constant amount.

12. A circuit as claimed in claim 10, wherein the phase adjustment means is responsive to successive interval signals to adjust the phase of the local clock by increasing amounts.

13. A circuit as claimed in claim 10, wherein the phase adjustment means is responsive to successive interval signals to adjust the phase of the local clock by reducing amounts.

14. A circuit as claimed in claim 10, wherein the phase adjustment means is responsive to successive interval signals to adjust the phase of the local clock by initially increasing then by reducing amounts.

15. A circuit as claimed in claim 1, wherein the timing means comprises a counter.

16. A circuit as claimed in claim 15, wherein the timing means is so arranged that the counter counts through a number of counts before issuing a timing signal.

17. A circuit as claimed in claim 16, wherein the timing means is so arranged that the counter begins a new count each time it issues a timing signal.

18. A circuit as claimed in claim 17, wherein the timing circuit is so arranged that each time a timing signal is issued, since the last data transition, the counter counts a respective number of counts in response to being loaded with a respective value stored in the circuit.

19. A circuit as claimed in claim 17, wherein the timing circuit is so arranged that the successive counts are smaller by a constant ratio to the previous one.

20. A circuit as claimed in claim 19, wherein the timing circuit is so arranged that after a certain number of successive counts the count becomes constant.

21. A circuit as claimed in claim 15 including an edge detect circuit for detecting a data transition on the first data channel and resetting in response the sequence of counts.

22. A circuit as claimed in claim 1 including an edge detect circuit for detecting a data transition on the first data channel and resetting in response the timing means.

23. A circuit as claimed in claim 1 including an edge detect circuit for detecting a data transition on the first data channel and resetting in response the phase of the local clock to that of the first data channel.

24. A circuit as claimed in claim 1, wherein the amount of the phase adjustments depends on the magnitude of the difference between the phase of the first data channel and said representative phase of said set.

25. A method of providing a local clock signal associated with a first data channel, the method comprising the steps of:

generating a local clock signal synchronised with the first data channel;

measuring the time since the last data transition on the first data channel and providing a timing signal indicative of that time;

detecting a phase representative of a selected set of one or more channels, that set comprising at least one channel other than the first data channel;

adjusting the phase of the local clock, in response to the timing signal, towards the phase of said set.

26. A method as claimed in claim 25, wherein said set consists of a single channel, that single channel being one of the channels other than the first data channel, and said representative phase is the phase of that single channel.

27. A method as claimed in claim 25, wherein said set comprises a plurality of channels.

28. A method as claimed in claim 27, wherein said phase representative of said set is an average of the phases of the members of said set.

29. A method as claimed in claim 27, wherein said set includes said first data channel.

30. A method as claimed in claim 25, wherein providing said timing signal comprises issuing a first interval signal when a first time period has elapsed since a last data transition occurred on the first data channel.

31. A method as claimed in claim 25, wherein providing said timing signal comprises issuing, in the continued absence of a data transition on the first data channel, interval signals at constant intervals.

32. A method as claimed in claim 25, wherein providing said timing signal comprises issuing, in the continued absence of a data transition on the first data channel, interval signals at intervals that get progressively shorter.

33. A method as claimed in claim 32 wherein the interval between successive interval signals gets smaller by a constant ratio.

34. A method as claimed in claim 32, wherein the intervals are subject to a minimum time interval.

35. A method as claimed in claim 30, wherein the step of adjusting the phase of the local clock occurs in response to said interval signals.

36. A method as claimed in claim 35, wherein the adjustment of the phase of the local clock occurs in constant amounts.

37. A method as claimed in claim 35, wherein the adjustment of the phase of the local clock occurs in increasing amounts.

38. A method as claimed in claim 35, wherein the adjustment of the phase of the local clock occurs in reducing amounts.

39. A method as claimed in claim 35, wherein the adjustment of the phase of the local clock occurs initially in increasing amounts and then in reducing amounts.

40. A method as claimed in claim 25 and further comprising the step of resetting the phase of the local clock to the phase of the first data channel in response to a data transition on that channel.

41. A method as claimed in claim 25 wherein the amount of the adjustments of the phase of the local clock depends on the magnitude of the difference between the phase of the first data channel and said representative phase of said set.